

**=> IFW: Scan as Doc Code: SRNT <=
 Doc Date:**

TC 3700 Inventor Search Program

See attached inventor searches for applications and/or patents to help resolve questions of overlapping subject matter. These searches are provided as an initial examination aid: examiners should perform updated or expanded PALM or EAST inventors searches as appropriate.

Serial Number:

09/538550

**1.) See attached printout of inventors listed in
PALM**

**2.) See attached EAST Inventor Search
Printout shows Inventor search terms**

US 20050272357 A1	US-PGPU	20051208	Sanding apparatus	451/355		Walker, Andrew
US 20050272356 A1	US-PGPU	20051208	Sanding apparatus	451/355		Walker, Andrew et al.
US 20050257385 A1	US-PGPU	20051124	Mode selection mechanism for power tool, and incorporating such mechanism	30/392		Walker, Andrew
US 20050222147 A1	US-PGPU	20051006	Process for the preparation of morpholine deriv intermediates therefore	514/232	514/235 544/140	Hayes, Martin Alistair et al.
US 20050220688 A1	US-PGPU	20051006	Exhaust system for an internal combustion eng	423/239	422/171 422/177	Allansson, Ronny et al.
US 20050128807 A1	US-PGPU	20050616	Nand memory array incorporating multiple ser devices and method for operation of same	365/185		Chen, En-Hsing et al.
US 20050122780 A1	US-PGPU	20050609	NAND memory array incorporating multiple w programming of individual memory cells and n operation of same	365/185		Chen, En-Hsing et al.
US 20050122779 A1	US-PGPU	20050609	Memory array incorporating memory cells arra strings	365/185		Fasoli, Luca G. et al.
US 20050081321 A1	US-PGPU	20050421	Hand-held cordless vacuum cleaner	15/344		Milligan, Michael A. et al.
US 20050079675 A1	US-PGPU	20050414	Semiconductor device with localized charge st and method of making same	438/261	257/324 257/E21 257/E29	Ilkbahar, Alper et al.
US 20050070060 A1	US-PGPU	20050331	TFT mask ROM and method for making same	438/200	257/E27 257/E27	Walker, Andrew J. et al.
US 20050069476 A1	US-PGPU	20050331	Selective catalytic reduction	423/239	422/171 422/177	Blakeman, Philip Gerald
US 20050062098 A1	US-PGPU	20050324	Storage layer optimization of a nonvolatile mer	257/324	257/325 257/E29 257/E29 438/261	Mahajani, Maitreyee et al.
US 20050052915 A1	US-PGPU	20050310	Nonvolatile memory cell without a dielectric at high- and low-impedance states	365/202		Herner, S. Brad et al.
US 20050023415 A1	US-PGPU	20050203	Spacecraft with extensible radiators	244/171	244/172	Walker, Andrew Nicholas
US 20040243858 A1	US-PGPU	20041202	Low power mode for device power managemen	713/300		Dennis, Lowell Browning
US 20040243631 A1	US-PGPU	20041202	System or method for gathering and utilizing in	707/104		Walker, Andrew S. et al.
US 20040214379 A1	US-PGPU	20041028	Rail stack array of charge storage devices and making same	438/149	257/E27 257/E27 257/E29 257/E29 257/E29	Lee, Thomas H. et al.
US 20040207001 A1	US-PGPU	20041021	Two mask floating gate EEPROM and method	257/314	257/E27 257/E27 257/E29 257/E29 257/E29 257/E29	Kouznetsov, Igor G. et al.
US 20040206996 A1	US-PGPU	20041021	Dense arrays and charge storage devices	257/296	257/E27 257/E27 257/E29 257/E29 257/E29 257/E29	Lee, Thomas H. et al.
US 20040159860 A1	US-PGPU	20040819	High density 3d rail stack arrays and method o	257/213	257/E21 257/E27 257/E27 257/E27	Patel, Kedar et al.
US 20040145024 A1	US-PGPU	20040729	NAND memory array incorporating capacitanc	257/390		Chen, En-Hsing et al.

			channel regions in unselected memory cells and operation of same			
US 20040128843 A1	US-PGPU	20040708	Support mechanism for a reciprocating tool	30/392	30/394	Walker, Andrew
US 20040125629 A1	US-PGPU	20040701	Programmable memory array structure incorporating connected transistor strings and methods for fabrication and operation of same	365/17		Scheuerlein, Roy E. et al.
US 20040124466 A1	US-PGPU	20040701	METHOD FOR FABRICATING PROGRAMMABLE MEMORY ARRAY STRUCTURES INCORPORATING SERIES-CONNECTED TRANSISTOR STRINGS	257/344	257/E21 257/E27	Walker, Andrew J. et al.
US 20040124415 A1	US-PGPU	20040701	Formation of thin channels for TFT devices to reduce variability of threshold voltages	257/65	257/E27 257/E29 257/E29	Walker, Andrew J. et al.
US 20040119122 A1	US-PGPU	20040624	Semiconductor device with localized charge storage and method of making same	257/390	257/E21 257/E21 257/E29	Ilkbahar, Alper et al.
US 20040098836 A1	US-PGPU	20040527	Handle assembly for tool	16/430		Walker, Andrew et al.
US 20040078936 A1	US-PGPU	20040429	Handle assembly for tool	16/430		Walker, Andrew et al.
US 20040069990 A1	US-PGPU	20040415	Thin film transistor with metal oxide layer and method of making same	257/66	257/E21 257/E27 257/E27 257/E27 257/E29 257/E29 438/158	Mahajani, Maitreyee et al.
US 20040044905 A1	US-PGPU	20040304	Data management system, method of providing data to database and security structure	726/19	707/9	Heath, John William et al.
US 20040036124 A1	US-PGPU	20040226	Inverted staggered thin film transistor with salicided source/drain structures and method of making same	257/382	257/383 257/390 257/E27 257/E27	Vyvoda, Michael A. et al.
US 20040000679 A1	US-PGPU	20040101	High density 3D rail stack arrays and method of making same	257/216	257/E21 257/E27 257/E27 257/E27	Patel, Kedar et al.
US 20030155582 A1	US-PGPU	20030821	Gate dielectric structures for integrated circuits and methods for making and using such gate dielectric structures	257/200	257/E29 257/E29 2006010 H01L31/00 M 20060 H01L C H01L31/00 CIPG 20 H01L31/00 M 20060 H01L C H01L31/00	Mahajani, Maitreyee et al.
US 20030070307 A1	US-PGPU	20030417	Power tool	30/374	30/393	Walker, Andrew
US 20030057435 A1	US-PGPU	20030327	Thin film transistors with vertically offset drain regions	257/135	257/E27 257/E27	Walker, Andrew J.
US 20030030074 A1	US-PGPU	20030213	TFT mask ROM and method for making same	257/204	257/347 257/E27	Walker, Andrew J. et al.
US 20030017796 A1	US-PGPU	20030123	Oscillating hand tool	451/357		Walker, Andrew
US 20030017795 A1	US-PGPU	20030123	Oscillating hand tool	451/356	451/357	Walker, Andrew
US 20020142546 A1	US-PGPU	20021003	Two mask floating gate EEPROM and method of making same	438/257	257/E27 257/E29	Kouznetsov, Igor G. et al.

					257/E29 257/E29 257/E29	
US 20020028541 A1	US-PGPU	20020307	Dense arrays and charge storage devices, and making same	438/149	257/E21 257/E21 257/E21 257/E27 257/E27 257/E29 257/E29 257/E29 257/E29	Lee, Thomas H. et al.
US 20020013708 A1	US-PGPU	20020131	Speech synthesis	704/260		Walker, Andrew et al.
US 20010055838 A1	US-PGPU	20011227	Nonvolatile memory on SOI and compound semiconductor substrates and method of fabrication	438/129	257/E21 257/E21 257/E27 257/E27 257/E27	Walker, Andrew J. et al.
US 7012299 B2	USPAT	20060314	Storage layer optimization of a nonvolatile memory	257/324	257/325 438/216	Mahajani; Maitreyee et al.
US 7005350 B2	USPAT	20060228	Method for fabricating programmable memory incorporating series-connected transistor strings	438/268	257/344	Walker; Andrew J. et al.
US 6992349 B2	USPAT	20060131	Rail stack array of charge storage devices and making same	257/324	438/261	Lee; Thomas H. et al.
US 6960794 B2	USPAT	20051101	Formation of thin channels for TFT devices to variability of threshold voltages	257/213	257/311 257/640	Walker; Andrew J. et al.
US 6940109 B2	USPAT	20050906	High density 3d rail stack arrays and method of	257/213	257/71; 257/E27 257/E27 257/E27	Patel; Kedar et al.
US 6897514 B2	USPAT	20050524	Two mask floating gate EEPROM and method of	257/314	257/296; 257/E29 257/E29 257/E29 257/E29	Kouznetsov; Igor G. et al.
US 6888750 B2	USPAT	20050503	Nonvolatile memory on SOI and compound semiconductor substrates and method of fabrication	365/185	257/E21 257/E21 257/E27 257/E27 257/E27	Walker; Andrew J. et al.
US 6881994 B2	USPAT	20050419	Monolithic three dimensional array of charge storage containing a planarized surface	257/296	257/74; 257/E21 257/E21 257/E27 257/E27 257/E29 257/E29 257/E29 257/E29	Lee; Thomas H. et al.
US 6875095 B2	USPAT	20050405	Oscillating hand tool	451/357	451/159	Walker; Andrew
US 6858899 B2	USPAT	20050222	Thin film transistor with metal oxide layer and making same	257/347	257/321; 257/E21 257/E27 257/E27 257/E27	Mahajani; Maitreyee et al.

					257/E29 257/E29	
US 6849905 B2	USPAT	20050201	Semiconductor device with localized charge storage and method of making same	257/390	257/391; 257/394; 257/E21 257/E29	Ilkbahar; Alper et al.
US 6841813 B2	USPAT	20050111	TFT mask ROM and method for making same	257/278	257/390; 257/E27 257/E27	Walker; Andrew J. et al.
US 6815781 B2	USPAT	20041109	Inverted staggered thin film transistor with salicide source/drain structures and method of making same	257/377	257/382; 257/390; 257/E27 257/E27	Vyvoda; Michael A. et al.
US 6780094 B2	USPAT	20040824	Oscillating hand tool	451/356	451/359	Walker; Andrew
US 6737675 B2	USPAT	20040518	High density 3D rail stack arrays	257/67	257/206; 257/369; 257/E21 257/E27 257/E27 257/E27	Patel; Kedar et al.
US 6692188 B1	USPAT	20040217	Rapid emergency dam and method of construction	405/115	210/162; 405/110	Walker; Andrew Gordon
US 6657241 B1	USPAT	20031202	ESD structure having an improved noise immunity and BICMOS semiconductor devices	257/173	257/174; 257/328; 257/357; 257/360; 257/546	Rouse; Mark W. et al.
US 6634169 B1	USPAT	20031021	Method and system for maintaining efficiency of catalyst	60/285	60/274;	Andersen; Paul Joseph et al.
US 6593624 B2	USPAT	20030715	Thin film transistors with vertically offset drain	257/344	257/324; 257/408; 257/E27 257/E27	Walker; Andrew J.
US 6479023 B1	USPAT	20021112	System for converting particulate matter in gas exhaust gases	422/186	204/164; 60/275	Evans; Julia Margaret et al.
US 6382636 B1	USPAT	20020507	Drill/driver chuck	279/60	279/140; 408/240	Walker; Andrew
US 6359316 B1	USPAT	20020319	Method and apparatus to prevent latch-up in CMOS	257/369	257/206; 257/373; 257/E27	Voss; Peter H. et al.
US 6011420 A	USPAT	20000104	ESD protection apparatus having floating ESD semiconductor structure	327/310	327/309; 327/453; 361/111; 361/56	Watt; Jeffrey et al.
US 5939028 A	USPAT	19990817	Combating air pollution	422/177	422/108; 422/170; 60/285; 60/311	Bennett; Stephen C et al.
US 5895950 A	USPAT	19990420	Semiconductor device having a non-volatile memory and method of manufacturing such a semiconductor device	257/315	257/316; 365/185	Walker; Andrew J. et al.
US 5828099 A	USPAT	19981027	Semiconductor device having a nonvolatile memory in which the floating gate is charged with hot charge from the source side	257/314	257/315	Van Dort; Maarten J. et al.
US 5816341 A	USPAT	19981006	Hammer mechanism	173/48	173/114; 173/201	Bone; Daniel et al.

US 5776417 A	USPAT	19980707	Emissions control	422/171	422/169; 422/177; 55/DIG. 60/320	Frost; Johnathan C. et al.
US 5751507 A	USPAT	19980512	KSD protection apparatus having floating EDS semiconductor structure	361/56	361/111	Watt; Jeffrey et al.
US 5743029 A	USPAT	19980428	Break-away cleat assembly for athletic shoes	36/134	36/114;	Walker; Andrew S. et al.
US 5682689 A	USPAT	19971104	Rotating cleats for athletic shoes	36/134	36/8.3	Walker; Andrew S. et al.
US 5617653 A	USPAT	19970408	Break-away cleat assembly for athletic shoe	36/134	36/128	Walker; Andrew S. et al.
US 5544274 A	USPAT	19960806	Electrical arrangement in power tools--power t switch	388/838	15/412; 200/61.7	Walker; Andrew et al.
US 5505012 A	USPAT	19960409	Directionally yieldable-cleat assembly	36/134	36/59C; 36/67A;	Walker; Andrew S. et al.
US 5395778 A	USPAT	19950307	Method of manufacturing an integrated circuit memory element	438/265	257/E21 438/593	Walker; Andrew J.
US 5377431 A	USPAT	19950103	Directionally yieldable cleat assembly	36/134	36/59C; 36/67A;	Walker; Andrew S. et al.
US 5371027 A	USPAT	19941206	Method of manufacturing a semiconductor dev non-volatile memory with an improved tunnel	438/264	257/E21 257/E21 257/E29 257/E29 438/766	Walker; Andrew J. et al.
US 5348843 A	USPAT	19940920	Method for making porcelain tags and signs by radiating a frit containing-emulsion coating app	430/275.	359/530; 430/198	Beck; Edward W. et al.
US 5286974 A	USPAT	19940215	Charged particle energy analyzers	250/305	250/306	Walker; Andrew R. et al.
US 4833081 A	USPAT	19890523	Bioreactor having cells in beads in a matrix	435/182	435/177;	Walker; Andrew G.
US 4818633 A	USPAT	19890404	Fibre-reinforced metal matrix composites	428/614	164/97;	Dinwoodie; John et al.
US 4810879 A	USPAT	19890307	Charged particle energy analyzer	250/305	250/306	Walker; Andrew R.
US 4420278 A	USPAT	19831213	Heading shield	405/301	299/31	Walker; Andrew J. et al.
US 4061979 A	USPAT	19771206	Phase locked loop with pre-set and squelch	455/260	331/17;	Walker; Andrew M. et al.
US 4000476 A	USPAT	19761228	Phase locked loop with circuit for preventing s	331/17	329/307; 331/23; 331/DIG 455/265	Walker; Andrew M. et al.
US 3945426 A	USPAT	19760323	Splash can for ingot molds and methods	164/137	249/206	Walker; Andrew et al.
US 3922496 A	USPAT	19751125	TDMA satellite communications system with g obviating ongoing propagation delay calculatio	370/324	375/356;	Gabbard; Ova Gene et al.
US 3564147 A	USPAT	19710216	LOCAL ROUTING CHANNEL SHARING S METHOD FOR COMMUNICATIONS VIA A RELAY	370/321	370/324; 455/13.2	Puente; John G. et al.